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Controlling memory effects of three-layer structured hybrid bistable devices based on graphene sheets sandwiched between two laminated polymer layers

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ABSTRACT

Three-layer structured hybrid bistable devices (HBDs) utilizing graphene sheets sandwiched between polymer layers were fabricated by laminating two glass substrates coated with patterned electrodes and spacers. The hybrid devices using polystyrene (PS) and poly (vinyl-carbazole) (PVK) as matrix layer for graphene sheets demonstrated write-once-read-many-time and volatile memory effects, respectively. It is found that the memory properties of the HBDs can be tailored by varying the depth of the charge traps formed between the polymer matrix and graphene sheets. The possible operating mechanisms of the HBDs were analyzed based on the investigation of current–voltage characteristics for the hybrid devices.

1. Introduction

Hybrid inorganic/organic nanocomposites containing inorganic nanomaterials have currently emerged as excellent candidates for potential applications in next-generation nonvolatile memory devices due to their high operating speed, high storage density, low power consumption and low fabricating cost [1–4]. So far various kinds of nanomaterials employed in nonvolatile memory devices utilizing hybrid inorganic/organic nanocomposites have been reported, such as C_{60} [5], granular metal nanoparticles [6], core/shell CdSe/ZnS nanoparticles [7], ZnO, In_2O_3, and NiFe nanoparticles [8–10]. However there have been relatively few reports on graphene sheets used in the hybrid memory devices. Graphene comprises one monolayer of carbon atoms packed into a two-dimensional honeycomb lattice [11,12]. Graphene's excellent mechanical and electrical properties, such as far superior mobility [13], thermal conductivity [14], current-carrying capabilities [15], and room temperature ballistic transport [16], combined with its compatibility with existing planar silicon-based technology, make it an attractive material for electric, optoelectronic, and photonic devices. Graphene sheets, acting as charging and discharging media, have been particularly interesting due to their being promising candidates for hybrid nanocomposites based nonvolatile memory devices.

This paper reports data for the fabrication and distinct memory effects of three-layer structured hybrid bistable devices (HBDs) utilizing graphene sheets sandwiched between polymer layers. As shown in Fig. 1, the sandwiched structure can avoid the contact uncertainty at the interface of electrode/hybrid layer induced from the single-layer structure reported by Zhuang [17], resulting in an improved operating stability of the HBDs. Furthermore, the polymer matrix-design approach allowed various polymer memories, including write-once read-many-time (WORM) memory and volatile memory to be realized. Scanning electron microscope (SEM) and atomic force microscope (AFM) measurements were performed to investigate the distribution of graphene sheets embedded in polymer

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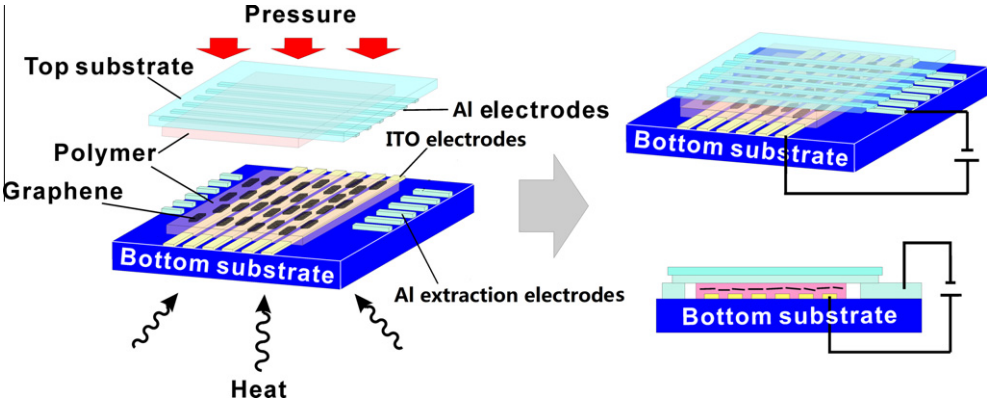

Fig. 1. Schematic diagram of the hybrid bistable memory devices fabricated utilizing graphene sheets sandwiched between polymer layers.

layers. Current–voltage (I–V) measurements were carried out to investigate the memory effects and the carrier transport behavior of the hybrid memory devices.

2. Experimental

As an active material, graphene sheets were prepared by reducing the colloidal suspension of exfoliated graphene oxide (GO) sheets in water with hydrazine hydrate, where GO sheets were prepared from purified natural graphite by the Hummers method [18]. The graphene powders were dispersed in deionized water (DI) and were sonicated until it became clear with no visible particulate matter. The polymer film used as a matrix layer in this work was formed by spin coating. In this work two kinds of polymer films were used: polystyrene (PS) and poly(vinyl-carbazole) (PVK). The two polymers were dissolved in chloroform with a concentration of 10 mg/mL.

For a multilayer structured device, conventional spin-coating technique would inevitably cause the destruction of underlying organic layer due to the presence of organic solvent. In this work, the three-layer structured HBDs were fabricated by laminating two glass substrates coated with patterned electrodes, which allowed multilayer structured devices to be realized without destroying the underlying polymer layer during spin-coating process. Fig. 1 shows the schematic of the fabrication process for the Al/polymer/graphene/polymer/ITO memory device, which contains two glass substrates, bottom substrate and top substrate. The top substrate coated by Al electrodes with a width of 1 mm and a thickness of 100 nm was prepared by conventional photolithography and a subsequent etching process. Typical ultrasonic cleaning processes with acetone, methanol, and DI water were performed to clean the top substrate. Then the polymer solution was spin coated onto the Al electrodes at 1200 rpm for 30 s. For bottom substrate, the ITO line electrodes with a width of 1 mm and a thickness of 200 nm were used. In particular, two lines of Al extraction electrode with a thickness of 250 nm were fabricated by thermal evaporation and a subsequent etching process, as shown in Fig. 1. The extraction electrode in the device have two functions: on one hand, they have electric connection to top Al electrodes when the two substrates are combined together. On the other hand, they can serve as spacers since the thickness of the active layer of polymer/graphene/polymer for the device could be adjusted exactly by controlling the thickness of the extraction electrodes. In previous works, the thickness of organic layer was controlled by the rotate speed of spin coating with unavoidable deviation. Here, the thickness of contact electrodes is 250 nm, thus the active layer of polymer/graphene/polymer between the bottom and top electrodes should be 50 nm-thick exactly. The bottom substrate was cleaned by typical ultrasonic cleaning processes, and a polymer layer was coated onto the electrodes by spin coating. After the evaporation of solvent, the bottom substrate was steeped into the graphene solution and was pulled slowly out of the solution, thus the graphene would paste on the substrate uniformly. The density and thickness of graphene sheets can be controlled by varying the concentration of graphene solution and the pulling speed. In this work the concentration of graphene solution is 10 mg/mL and the pulling speed is 1 cm/min. The bottom electrodes are perpendicular to the top electrodes, and the top electrodes were connected to the extraction electrodes. Then the top substrate was pressed on the bottom substrate, and heated to 130 °C with a pressure for 30 min, as shown in Fig. 1.

Field-emission scanning electron microscope (FE-SEM, NOVA nanoSEM-230) and AFM (Vecoo NanoScope IIIa) was used to investigate the distribution and thickness of graphene sheets embedded in polymer layers. I–V measurements on the HBDs were performed at room temperature using a semiconductor characterization system (Keithley 4200-SCS).

3. Results and discussion

3.1. Morphology of graphene sheets deposited on polymer layer

Fig. 2a shows a FE-SEM image of the graphene film deposited on PS layer. It is shown that the film has a high graphene density and uniform morphology. A high-magnification FE-SEM image, as shown in inset of Fig. 2a, indicates that the graphenes are consistently oriented, and all of them are almost in parallel with the substrate

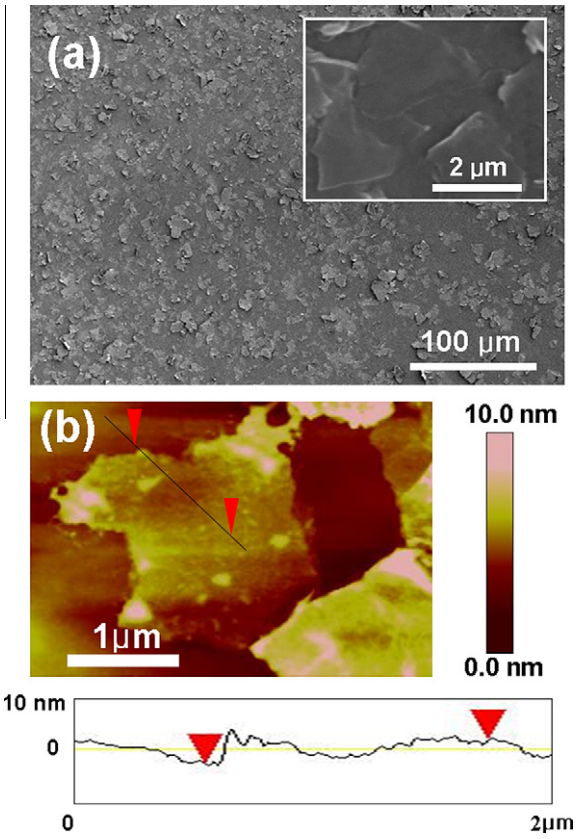

Fig. 2. (a) FE-SEM image of graphene sheets deposited on PS layer. The inset is a magnified FE-SEM image of graphene sheets on PS layer. (b) AFM image of graphene sheets and the bottom section is the cross-sectional analysis.

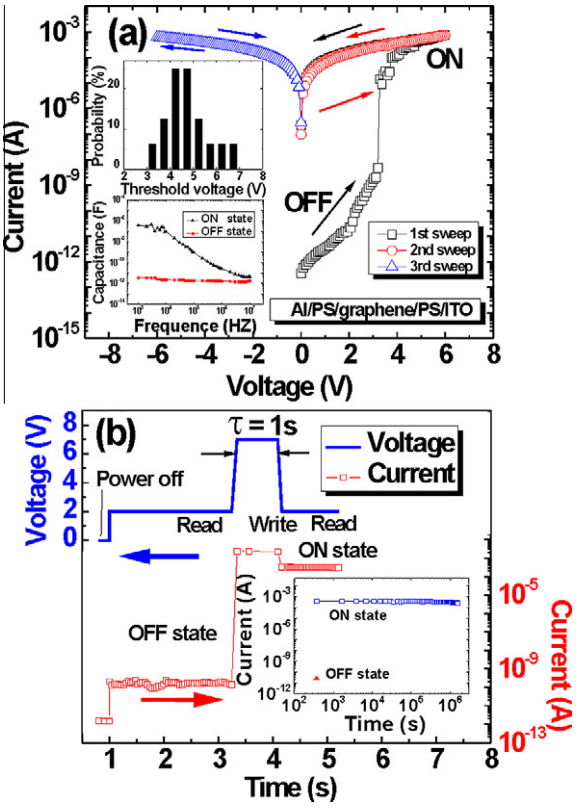

Fig. 3. (a) I–V curves for the Al/PS/graphene/PS/ITO memory device. The inset is the probability of the "write" voltage distributions (top) and frequency dependence of capacitance in both the ON and OFF states (bottom). (b) I–V characteristics of "read–write–read" sequence test. And the inset is the result of retention test for 10^6 s.

due to their good flexibility. Fig. 2b is an AFM image of the graphene sheets deposited on PS layer, and the bottom of Fig. 2b shows a cross-sectional analysis of the selected region between the two arrows shown in the top of Fig. 2b. The thickness of the graphene sheets layer is estimated to be about 3 nm.

3.2. WORM memory effect for Al/PS/graphene/PS/ITO device

In the current–voltage measurement, the top Al electrode is set as 0 V and the bias is applied to the bottom ITO electrode. Fig. 3a shows I–V curves for the Al/PS/graphene/PS/ITO memory device measured at room temperature. The device clearly shows counterclockwise electrical hysteresis behavior, an essential feature of bistable memory device. Two distinct conducting states are observed: a relatively high-current state (ON state) and a relatively low-current state (OFF state). During the first forward direction voltage sweep, an original low current was observed for the device in a bias range from 0 V to 3.2 V. A sharp increase in the current, from 10^{-9} A to 10^{-5} A, took place at around 3.2 V, indicating the transition for the memory device from OFF state to ON state. After the transition, the current gradually increased in the bias range from 3.2 V to 6 V, and the current remain at around 10^{-4} A. The maximum current ratio between the ON and the OFF state for the Al/PS/graphene/PS/ITO memory device at 2 V bias ("read" voltage) is as large as about 1×10^7. After the transition from OFF state to ON state, the device remains in high-current state, as shown in the subsequent sweep from 6 V to 0 V. In the second sweep from 0 V to 6 V and from 6 V to 0 V, the device still remains at ON state, indicating the nonvolatile properties of the Al/PS/graphene/PS/ITO memory device. In the third voltage sweep from 0 V to −6 V or even larger reverse bias, as shown in Fig. 3a, no decrease in current was observed, indicating the device is a write-once-read-many-times (WORM) memory device.

It is important to investigate the device-to-device uniformity of organic memory devices. 16 out of 25 cells (64%) operated properly in 5×5 memory cell arrays, suggesting the high reproducibility of the device. The top inset of Fig. 3a shows the probability of the "write" voltage distributions extracted from I–V plots. The distribution of the "write" voltage is between 3 V and 7 V. Thus for Al/PS/graphene/PS/ITO device, the "write" voltage can be set as 7 V.

The capacitance of the Al/PS/graphene/PS/ITO device was measured at the ON-state and the OFF-state, respectively, as shown in the bottom inset of Fig. 3a. The device at the OFF state exhibits a capacitance of $\sim 10^{-12}$ F from 1 k Hz to

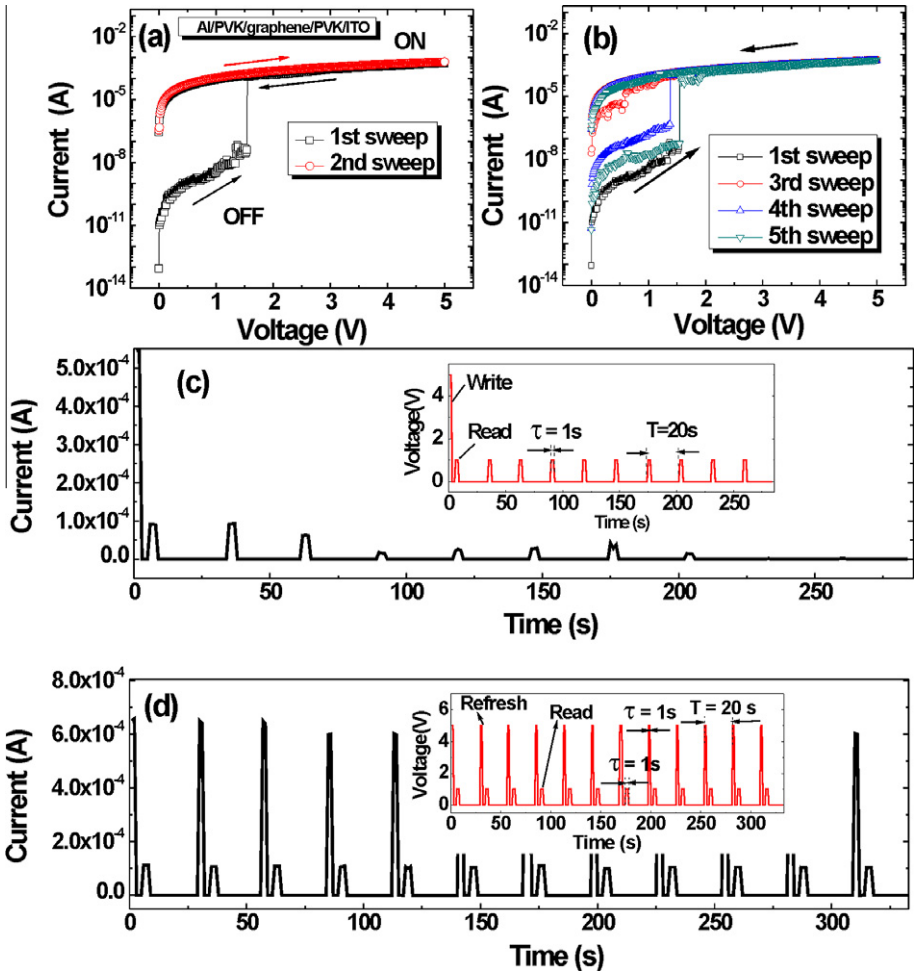

Fig. 4. Electrical properties for Al/PVK/graphene/PVK/ITO memory device (a) and (b) show I–V curves for the memory device under sequent voltage sweeps (c) and (d) show the results of retention test without and with refresh pulse.

10^7 Hz, which is insensitive to the frequency, while the capacitance shows strong dependence on the frequency when the device is at the ON state. For the device at the ON state, the capacitance at high frequency is almost the same as that at the OFF state, while it gradually increases with the decrease of the frequency. The result suggests that no dielectric breakdown took place in the PS/graphene/PS active layer when the device at ON the state [19]. It should be noted that the device at the ON state shows a capacitance five orders of magnitude higher than that at the OFF state at low frequency. The capacitance difference may be partly caused by the increase in the dielectric constant of the PS/graphene/PS layer. It is believe that the change of the dielectric constant of the layer may be associated with the field-induced dipole formation, indicative of charges trapping for the device at the ON-state [20].

In a WORM device, writing of each cell is achieved via a voltage pulse to "switch" the cell from OFF state to ON state. Once writing is completed, the cell will remain at the ON state and can be "read" many times. Fig. 3b depicts "writing" and "reading" processes on an Al/PS/graphene/PS/ITO memory device cell as an example. A "read–write–read" sequence pulse was applied and the current is recorded, as shown in Fig. 3b. In the beginning, a 2 V positive voltage of pulse ("read" voltage) was applied to a memory unit to read the initial OFF state. The OFF state could be detected with a current of $\sim 10^{-11}$ A. Then, a 7 V voltage of pulse ("write" voltage) was given to the unit to switch the device from OFF state to ON state. After this "write" process, the "read" voltage was again applied to read the ON state of this memory device. This ON state could be detected with a current of $\sim 10^{-4}$ A. During the test time of 1×10^6 s the current at the ON state is stable only with a little reduction, as shown in the inset of Fig. 3b. The result indicates that the memory device exhibited excellent environmental stability in ambient conditions.

3.3. Volatile memory effect for Al/PVK/graphene/PVK/ITO device

To realize the volatile memory effect, PVK was used as matrix layer for graphene sheets. The memory effect for Al/PVK/graphene/PVK/ITO memory device is shown in Fig. 4a. The device is swept with a voltage step of 0.05 V in a cycle from 0 to 5 V and then from 5 to 0 V. In the first sweep from 0 to 5 V, an abrupt increase in current is ob-

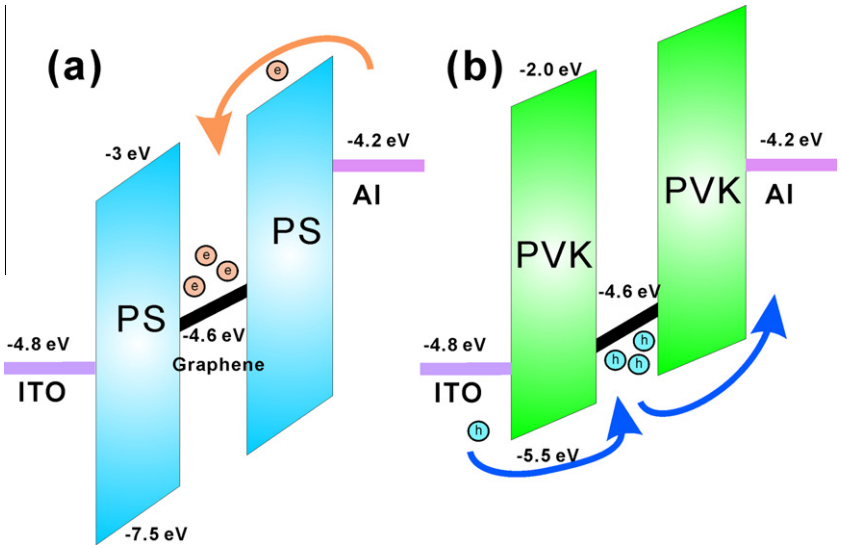

Fig. 5. Schematics of the electronic structures corresponding to the operating mechanisms of the charge-capturing and the charge-storing processes for (a) Al/PS/graphene/PS/ITO memory device, (b) Al/PVK/graphene/PVK/ITO memory device. The work function of graphene is taken from Ref. [22], HOMO and LUMO of PS and PVK are taken from Ref. [23].

served at a threshold voltage of about 1.5 V, indicating the conductance transition from the OFF state to the ON state ("write" process). The device remained in ON state during the subsequent reverse direction scan. The distinct bistable states in the voltage range of 0–1.5 V allowed a voltage (e.g., 1 V) to read the OFF and ON signal of the memory. The maximum current ratio between the ON and the OFF state for the Al/PVK/graphene/PVK/ITO device at 1 V bias is as large as 1×10^4. In the second sweep (immediately following the first sweep) from 0 to 5 V and subsequent reverse direction scan, the device remained at the ON state, as shown in Fig. 4a. The third sweep is conducted after turning off the power for about 20 s. It is found that the device almost remained at the ON state only with a little reduction. After turning off the power for 60 s, the fourth sweep is carried out, as shown in Fig. 4b. The device relaxes to relative low current state ($\sim 10^{-7}$ A) at low bias, and the abrupt increase of current also occurred at 1.5 V. After turning off the power for 120 s the fifth sweep is carried out. The device almost returned to its original state with a low current of about 10^{-8} A and the electrical behavior was similar to the first sweep. This indicates that the ON state for the Al/PVK/graphene/PVK/ITO device is unstable, and can relax to the steady OFF state without an erasing process. The short retention time of the ON state indicates that the memory device is volatile.

To reveal the relaxing process from ON state to the steady OFF state, the Al/PVK/graphene/PVK/ITO device was firstly written to ON state with a bias of 5 V, then a read voltage pulse of 1 V in every 20 s was applied to read the current state. As shown in Fig. 4c, after ~180 s the current under read bias was almost reduced to undistinguished state. However, the ON state can be electrically sustained by a refreshing voltage pulse of 5 V in every 20 s, as shown in Fig. 4d. This ability to write, read and refresh the electric states of the device fulfills the functionality of a volatile memory.

3.4. Mechanisms for controlling memory effect of Al/polymer/graphene/polymer/ITO devices

The operating mechanism of resistive-switch for polymer/graphene/polymer devices may be due to the charges capture in graphene sheets. The graphene sheets act as traps, capturing carriers injected from the electrode. The carriers captured in the graphene generate a strong local internal field inside the organic layer, which enables the organic layers to undergo a conductance change upon bias [21]. The depth of traps plays a key role in determining the type of memory effect of the hybrid devices. In this study the depth of traps is modulate by utilizing different polymer. The highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) for PS are −7.5 eV and −3 eV, respectively. For PS/graphene/PS active layer, the energy difference between the work function of the Al and LUMO of the PS (1.2 eV) is much lower than that between the work function of the ITO and HOMO of the PS (2.7 eV). The difference in the work functions favors electron injection over hole injection from the Al electrodes into the LUMO of PS layer, and the injected electrons can be captured by graphene sheets, as shown in Fig. 5a. The electron traps formed between graphene and PS are deep (1.6 eV) that the captured electrons cannot release even under a big reverse bias, which exhibits WORM memory effect. For PVK the HOMO and LUMO are −5.5 eV and −2.0 eV, respectively. The energy difference between the work function of the ITO and the HOMO of the PVK (0.7 eV) is much lower than that between the work function of the Al and LUMO of the PVK (2.2 eV), thus the holes are injected from the ITO into the HOMO of PVK layer. Once the injected holes meet the graphene sheets they can be captured. For the PVK-based device, the traps are shallow (0.9 eV) that the captured holes could be released by thermal agitation, as shown in Fig. 5b, and the volatile memory effect is shown.

4. Conclusions

Hybrid bistable memory devices based on graphene sheets sandwiched between two polymer layers was fabricated by laminating two glass substrates coated with patterned electrodes, which allowed multilayer structured devices to be realized without destroying the underlying polymer layer during spin-coating process. By using PS and PVK as organic matrix layer for graphene sheets, the hybrid bistable devices demonstrated WORM and volatile memory effects, respectively. The distinct electrical behavior is proposed to be related to the different depth of charge traps formed between the graphene sheets and polymer matrix, which provides a new route to tailor the memory effects of the hybrid bistable devices. The results show that hybrid bistable memory containing graphene sheets sandwiched between polymer layers holds promise for potential applications in next-generation flash memories.

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References

[1] H.I. Hanafi, S. Tiwari, I. Khan, Fast and long retention-time nanocrystal memory, IEEE Trans. Elect. Dev. 43 (1996) 553.
[2] J. Blauwe, Nanocrystal nonvolatile memory devices, IEEE Trans. Nanotechnol. 1 (2002) 2.
[3] S.S. Kim, W.J. Cho, C.G. Ahn, K. Im, J.H. Yang, I.B. Baek, S. Lee, K.S. Lim, Fabrication of fin field-effect transistor silicon nanocrystal floating gate memory using photochemical vapor deposition, Appl. Phys. Lett. 88 (2006) 223502.
[4] T.Z. Lu, M. Alexe, R. Scholz, V. Talelaev, M. Zacharias, Multilevel charge storage in silicon nanocrystal multilayers, Appl. Phys. Lett. 87 (2005) 202110.
[5] S. Cho, D. Lee, J. Jung, T. Kim, Electrical bistabilities and memory stabilities of nonvolatile bistable devices fabricated utilizing C_{60} molecules embedded in a polymethyl methacrylate layer, Nanotechnology 20 (2009) 345204.
[6] L.D. Bozano, B.W. Kean, V.R. Deline, J.R. Salem, J.C. Scott, Mechanism for bistability in organic memory elements, Appl. Phys. Lett. 84 (2004) 607.
[7] F. Li, S.H. Cho, D.I. Son, K.H. Park, T.W. Kim, Multilevel nonvolatile memory effects in hybrid devices containing CdSe/ZnS nanoparticle double arrays embedded in the C_{60} matrices, Appl. Phys. Lett. 92 (2008) 102110.
[8] D.I. Son, C.H. You, J.H. Jung, T.W. Kim, Carrier transport mechanisms of organic bistable devices fabricated utilizing colloidal ZnO quantum dot-polymethylmethacrylate polymer nancomposites, Appl. Phys. Lett. 97 (2010) 013304.
[9] H.M. Koo, W.J. Cho, D.U. Lee, S.P. Kim, E.K. Kim, Improvement of charge storage characteristics on floating gated nonvolatile memory devices with In_2 O_3 nanoparticles embedded polyimide gate insulator, Appl. Phys. Lett. 91 (2007) 043513.
[10] J.H. Jung, J.H. Kim, T.W. Kim, C.S. Yoon, Y.H. Kim, S. Jin, Nonvolatile memory cell effect in multilayered Ni_{1-x} Fe_x self-assembled nanoparticles arrays in polyimide, Appl. Phys. Lett. 89 (2006) 022112.
[11] A.K. Geim, K.S. Novoselov, The rise of graphene, Nat. Mater. 6 (2007) 183.
[12] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Grigorieva, I.V. Dubonos, A.A. Firsov, Electric field effect in atomically thin carbon films, Science 306 (2004) 666.
[13] Y.B. Zhang, Y.W. Tan, H.L. Stormer, P. Kim, Experimental observation of the quantum hall effect and berry's phase in graphene, Nature (London) 438 (2005) 201.
[14] A.A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, C.N. Lau, Superior thermal conductivity of single-layer graphene, Nano Lett. 8 (2008) 902.
[15] J. Moser, A. Barreiro, A. Bachtold, Current-induced cleaning of graphene, Appl. Phys. Lett. 91 (2007) 163513.
[16] M. Muller, M. Brauninger, B. Trauzettel, Temperature dependence of the conductivity of ballistic graphene, Phys. Rev. Lett. 103 (2009) 196801.
[17] X. Zhuang, Y. Chen, G. Liu, P. Li, C. Zhu, E. Kang, K. Noeh, B. Zhang, J. Zhu, Y. Li, Conjugated-polymer-functionalized graphene oxide: Synthesis and nonvoltatile rewritable memory effect, Adv. Mater. 22 (2010) 1731.
[18] W. Hummers, R. Offeman, Preparation of graphitic oxide, J. Am. Chem. Soc. 80 (1958) 1339.
[19] C.W. Chu, J. Ouyang, J. Tseng, Y. Yang, Organic donor–acceptor system exhibiting electrical bistability for use in memory devices, Adv. Mater. 17 (2005) 1440.
[20] L. Ma, S. Pyo, J. Ouyang, Q. Xu, Y. Yang, Nonvolatile electrical bistability of organic-metal-nanocluster-organicsystem, Appl. Phys. Lett. 82 (2003) 1419.
[21] D.I. Son, T.W. Kim, J.H. Shim, J.H. Jung, D.U. Lee, J.M. Lee, W. Park, W.K. Choi, Flexible organic bistable devices based on graphene embedded in an insulating poly(methyl methacrylate) polymer layer, Nano Lett. 10 (2010) 2441.
[22] J.W.G. Wildoer, L.C. Venema, A.G. Rinzler, R.E. Smalley, C. Dekker, Electronic structure of atomically resolved carbon nanotubes, Nature 391 (1998) 59.
[23] F. Li, D.I. Son, B.J. Kim, T.W. Kim, Nonvolatile electrical bistability and operating mechanism of memory devices based on CdSe/ZnS nanoparticle/polymer hybrid composites, Appl. Phys. Lett. 93 (2008) 021913.